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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,902	03/30/2004	Shoichiro Chiba	XA-10064	1331

181 7590 05/10/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/811,902	CHIBA ET AL.
	Examiner	Art Unit
	Gene N. Auduong	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-30-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on March 30, 2004 is being considered by the examiner.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikehashi et al. (U.S. Pat. No. 6,643,180).

Regarding claim1, Ikehashi et al. disclose a semiconductor memory device with test mode comprising: a plurality of internal circuits (figure 1) including a nonvolatile memory and a central processing unit (figure 1, nonvolatile memory array 11 and controller 25), wherein the nonvolatile memory comprises a memory array including electrically erasable and writable

nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film (col. 8, lines 61+), wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and wherein the data read from the specific storage region is repair information for replacing a normal storage region in a predetermined internal circuit with a redundant storage region in the predetermined internal circuit (defective address column register 19 for storing repair information for the device; col. 9, lines 38+).

Regarding claim 2, Ikehashi et al. disclose a semiconductor memory device with test mode comprising: a plurality of internal circuits (figure 1) including a nonvolatile memory and a central processing unit (figure 1, nonvolatile memory array 11 and controller 25), wherein the nonvolatile memory comprises a memory array including electrically erasable and writable nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film (col. 8, lines 61+), wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and wherein the data read from the specific storage region is trimming information for adjusting characteristics of a predetermined internal circuit (trim data register 21 and trim data register 23 for storing repair information for the device; col. 9, lines 59+).

Regarding claim 3, Ikehashi et al. disclose a semiconductor memory device with test mode comprising: a plurality of internal circuits (figure 1) including a nonvolatile memory and a central processing unit (figure 1, nonvolatile memory array 11 and controller 25), wherein the

nonvolatile memory comprises a memory array 11 including electrically erasable and writable nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film (col. 8, lines 61+), and wherein the data processor (control logic 25) comprises an input terminal of an operation mode signal for selectively designating a first mode of allowing a predetermined internal circuit to control rewriting of information stored in the nonvolatile memory or a second mode of allowing an external device connected to the data processor to control the rewriting (co. 10, lines 11+).

Regarding claim 13, Ikehashi et al. disclose a semiconductor device comprising: a plurality of internal circuits including a nonvolatile memory and a central processing unit (control logic 25), and an input terminal of an operation mode signal (I/O control 24) for selectively designating a first mode of allowing a first internal circuit to control rewriting of information stored in the nonvolatile memory or a second operation mode of allowing an external device coupled to the data processor to control the rewriting, wherein the nonvolatile memory comprises a memory array 11 including electrically erasable and writable nonvolatile memory cells (NAND type flash memory cells), each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film, wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and wherein the data read from the specific storage region includes: repair information for replacing a normal storage region in a second internal circuit

with a redundant storage region in the second internal circuit, and trimming information for adjusting characteristics of a third internal circuit (col. 9, lines 29+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi et al. (U.S. Pat. No. 6,643,180).

Regarding claims 4-12, Ikehashi et al. disclose the device having all of the limitation according to claim 1. Ikehashi et al. do not specifically disclose wherein the nonvolatile memory cell comprises a first transistor part used for storing information and a second transistor part for selecting the first transistor part, wherein the first transistor part is of an MONOS type including the charge storage insulating film and a memory gate electrode, and wherein the second transistor part is of an MOS type; wherein a channel region of the first transistor part and a channel region of the second transistor part are adjacent to each other, and wherein a gate insulating withstand voltage of the second transistor part is lower than that of the first transistor part; wherein the first transistor part includes a source line electrode connected to a source line, the memory gate electrode connected to a memory gate control line, and the charge storage insulating film disposed directly below the memory gate electrode, and wherein the second transistor part includes a bit line electrode connected to a bit line and a control gate electrode connected to a control gate control line; a switch MOS transistor capable of coupling the bit line

to a global bit line, wherein a gate oxide film of the switch MOS transistor is thinner than that of the first transistor part; a first driver for driving the control gate control line; a second driver for driving the memory gate control line; a third driver for driving the switch MOS transistor to an on state; and a fourth driver for driving the source line, wherein the first and third drivers use a first voltage as an operation power source, and the second and fourth drivers use a voltage higher than the first voltage as an operation power source and its functioning characteristic. However, it's obvious and known to one of ordinary skill in the art to understand that NAND type flash memory as used in the device is one type of nonvolatile memory cells, and its can be replaced with any other cell structure base on the need and structuring of the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ikehashi's device to replace NAND type memory cells with the cells structure as claimed based on the device structure and best used cells type in particular device to obtain the highest performance.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
April 20, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827